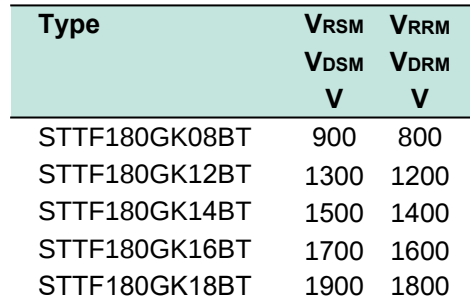


Fast Thyristor-Thyristor Modules



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Sirectifier®

STTF180GK16BT

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Symbol	Test Conditions	Characteristic Values	Unit
I_{RRM}, I_{DRM}	$T_{VJ}=T_{VJM}; V_R=V_{RRM}; V_D=V_{DRM}$	5 0	mA
V_T, V_F	$I_T, I_F=540A; T_{VJ}=25^{\circ}C$	1.90	V
V_{TO}	For power-loss calculations only ($T_{VJ}=125^{\circ}C$)	1.30	V
r_T		0.90	mΩ
V_{GT}	$V_D=6V;$ $T_{VJ}=25^{\circ}C$ $T_{VJ}=-40^{\circ}C$	2.2 2.4	V
I_{GT}	$V_D=6V;$ $T_{VJ}=25^{\circ}C$ $T_{VJ}=-40^{\circ}C$	250 300	mA
V_{GD}	$T_{VJ}=T_{VJM}; V_D=2/3V_{DRM}$	0.25	V
I_{GD}		10	mA
I_L	$T_{VJ}=25^{\circ}C; t_p=30\mu s; V_D=6V$ $I_G=0.5A; di_G/dt=0.5A/\mu s$	1000	mA
I_H	$T_{VJ}=25^{\circ}C; V_D=6V; R_{GK}=\infty$	250	mA
t_{gd}	$T_{VJ}=25^{\circ}C; V_D=1/2V_{DRM}$ $I_G=0.5A; di_G/dt=0.5A/\mu s$	1.2	μs
t_q	$T_{VJ}=T_{VJM}; I_T=300A; t_p=200\mu s; -di/dt=10A/\mu s$ $V_R=100V; dv/dt=20V/\mu s; V_D=2/3V_{DRM}$	18-25	μs
Q_s	$T_{VJ}=T_{VJM}; I_T, I_F=300A; -di/dt=50A/\mu s$	550	μC
I_{RM}		235	A
R_{thJC}	per thyristor/diode; DC current per module	0.130 0.065	K/W
R_{thJK}	per thyristor/diode; DC current per module	0.225 0.1125	K/W
d_s	Creeping distance on surface	12.7	mm
d_A	Strike distance through air	9.6	mm
a	Maximum allowable acceleration	50	m/s ²

FEATURES

- * International standard package
- * Copper baseplate
- * Pressure Contact Technology
- * Isolation voltage 3600 V~
- * RoHS compliant

APPLICATIONS

- * Motor control
- * Power converter
- * Heat and temperature control for industrial furnaces and chemical processes
- * Lighting control
- * Contactless switches

ADVANTAGES

- * Space and weight savings
- * Simple mounting
- * Improved temperature and power cycling
- * Reduced protection circuits



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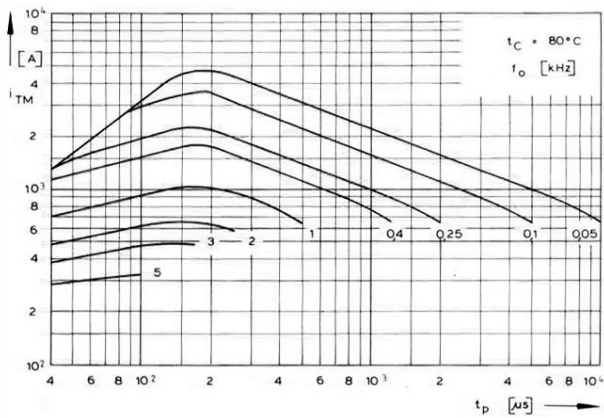


Fig.1 Maximum allowable current load versus halfwave duration per arm at: sinusoidal current waveform, given case temp. t_c , forward off-state voltage $V_{DM} \leq 2/3 V_{RRM}$

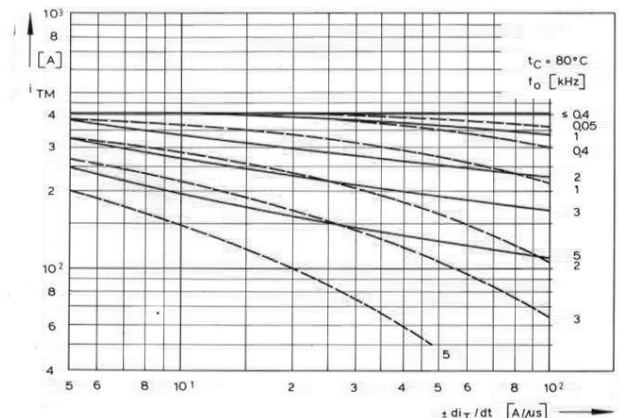


Fig.2 Maximum allowable current load versus rate of current per arm at: trapezoidal current waveform, given case temp. t_c , forward off-state voltage $V_{DM} \leq 2/3 V_{RRM}$

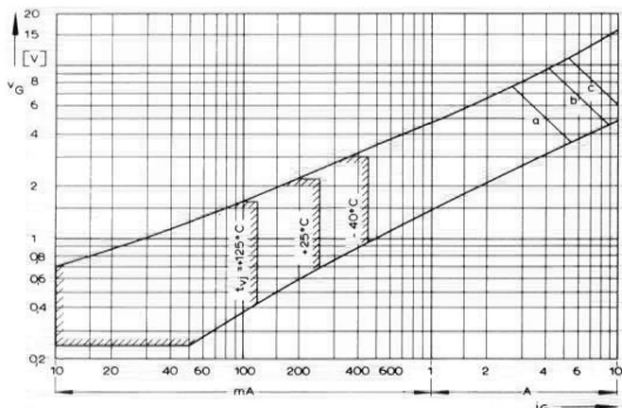


Fig.3 Gate characteristic and peak gate power dissipation at $V_D = 6\text{V}$

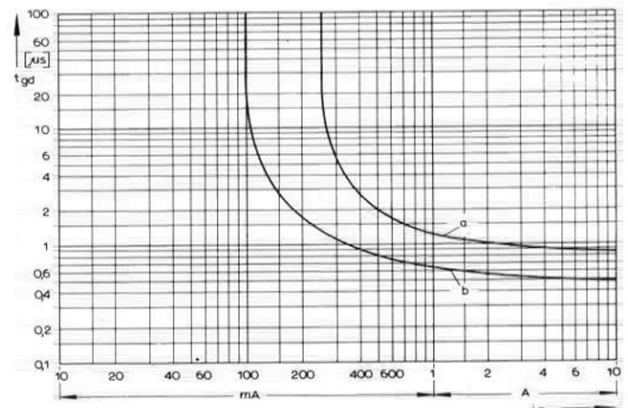


Fig. 4 Gate controlled delay time t_{gd} , $t_a = 1\mu\text{s}$, $t_{vj} = 25^\circ\text{C}$
a=Limiting characteristic b=Typical characteristic

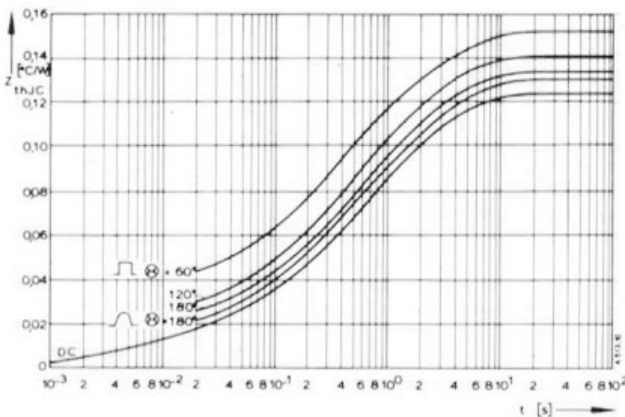


Fig.5 Transient thermal impedance per arm Z_{thJC} , Junction to case

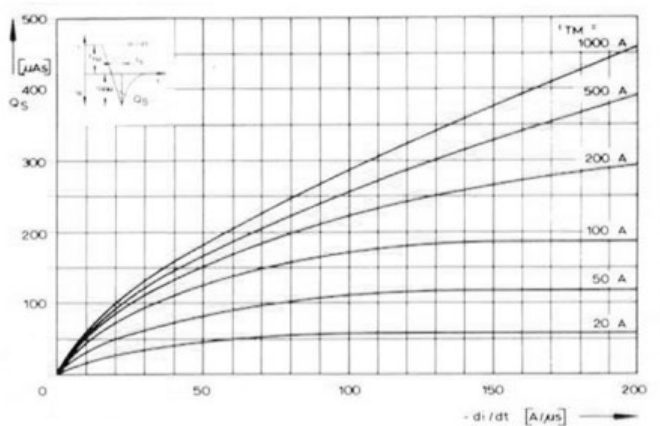


Fig.6 Typical relationship between the maximum lag charge Q_s and the rate of decay of on-state current $-di_T/dt$ at t_{Vjmax}